AMENDMENTS TO DRAWINGS

The attached sheet of drawings includes changes to FIG. 5A.

Attachment: Replacement sheet

REMARKS

Claims 15-19 were previously withdrawn. Claims 13, 37, 38, and 40-59 were previously canceled. Claims 1, 20, 25, and 39 have been amended to correct typographical errors and for clarification purposes. Claims 1-12, 14, 20-36, 39, 60-69 are pending in this application. No new matter has been added. Applicant gratefully acknowledges the statement by the Examiner that claims 20-24 are allowed.

The specification has been editorially revised. Figure 5A of the drawings has been amended to correct a typographical error.

Claims 1-3, 25-27, 64, 65, 67, and 68 stand rejected under 35 U.S.C. § 102(e) as being anticipated by Kozlowski et al. (U.S. Pat. No. 6,498,331). This rejection is respectfully traversed.

Claim 1 recites, *inter alia*, "[a] pixel cell comprising" "at least one transistor structure is configured to have at least two threshold voltages associated with the at least one channel region, and wherein a current-voltage characteristic of the transistor structure is determined at least in part by the threshold voltages." Similarly claim 25 recites, *inter alia*, "[a]n image sensor comprising" "the transistor structure is configured to have at least two threshold voltages associated with the at least one channel region, and wherein an current-voltage characteristic of the transistor structure is determined at least in part by the threshold voltages."

Kozlowski relates to an apparatus and method for achieving uniform low dark currents by setting "[a] threshold voltage of a reset FET in an active pixel sensor ... to an appropriate value such that the dark current from a photodiode is actively removed through the reset FET." (Kozlowski, col. 1, lines 59-63). More specifically, Kozlowski teaches that "if the threshold voltage V_t of the reset FET 14 is set

appropriately, the dark current I_{DK} 24 can be "siphoned off" (i.e. subtracted) through the reset FET 14 as the photocurrent is also integrated." (Kozlowski, col. 3, lines 20-23, FIG. 1).

The Examiner states Kozlowski discloses that "at least one reset transistor 14 has at least two threshold voltages (at 0.5v, 0.8v, or 1v in Fig 2)." (Office Action, page 3). Applicant respectfully disagrees. In Figure 2, Kozlowski "shows a graph of detector dark current vs. optimum threshold voltage for 0.5um CMOS." (Kozlowski, col. 3, lines 33-36). Kozlowski's Figure 2 does not disclose a reset transistor having two threshold voltages. Instead, Figure 2 illustrates how much dark current will be detected based upon a particular value (0.5v, 0.8v, 1v, etc.) set for the single threshold voltage (V_t) of the reset FET.

The Examiner further states that Kozlowksi discloses that "an I-V characteristic of the reset transistor 14 is determined at least in part by the threshold voltages." (Office Action, page 3). Applicant respectfully disagrees. Kozlowski discloses that "in a typical prior art design, the standard threshold voltage V_t of the reset FET 14 for a 0.5um CMOS process was on the order of 0.55 volts." (Kozlowski, col. 3, lines 24-27). Kozlowski further discloses that "[t]his value was chosen by prior art CMOS processes in order to maximize the dynamic range at low supply voltages for general digital circuits." (Kozlowski, col. 3, lines 27-29). Kozlowski does not teach or disclose the "current-voltage characteristic of the transistor structure ... [being] determined at least in part by [the at least two] threshold voltages," as recited by claims 1 and 25.

As discussed, Kozlowski fails to teach or disclose a transistor structure configured to have at least two threshold voltages, as recited by claims 1 and 25. Kozlowski refers to one threshold voltage V_t associated with a reset transistor being set

to one of a range of values in order to uniform low dark currents. Kozlowski fails to teach or disclose all limitations of claims 1 and 25; therefore, claims 1 and 25 are allowable.

Claims 2, 3, 64 and 65 depend from claim 1 and are allowable for at least the reasons stated above. Applicant respectfully requests the withdrawal of the rejection and the claims allowed.

Claims 26 and 27 depend from claim 25 and are allowable for at least the reasons stated above. Applicant respectfully requests the withdrawal of the rejection and the claims allowed.

Claims 67 and 68 depend from claim 20. As the Examiner has stated that claim 20 is allowable, Applicant respectfully assumes that the rejection was in error. As such, Applicant respectfully requests the withdrawal of the rejection and the claims allowed.

Claims 4, 7 11, 12, 14, 28, 31, 36, 39, 60-63, 66, and 69 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over Kozlowski et al. (U.S. Pat. No. 6,498,331). This rejection is respectfully traversed.

As previously discussed, Kozlowski fails to disclose, teach or suggest every limitation of claims 1 and 25. Claim 39 recites similar limitations as claims 1 and 25. Claim 39 recite, *inter alia*, "a processor system comprising" "the transistor structure ... [being] configured to have at least two threshold voltages associated with the at least one channel region, and wherein an current-voltage characteristic of the transistor structure is determined at least in part by the threshold voltages."

Kozlowski fails to teach or suggest the limitations, as discussed above. The Examiner cites Hynecek (U.S. Pat. No. 5,546,438), Koizumi et al. (U.S. Pat. Pub. 2003/0137594), Guidash (U.S. Pat. No. 6,504,195), and Sakuragi et al. to support what the Examiner indicates are well known positions. None of these references; however, supplement the deficiencies of Kozlowski. For at least the reasons discussed above, claim 39 is non-obvious over Kozlowski and therefore is allowable.

Claims 4, 7, 11, 12, 14, and 66 depend from claim 1 and contain all of its limitations. For at least the reasons stated above, Applicant respectfully requests the withdrawal of the rejection and allowance of the claims.

Claims 28, 31, 35, 36, and 63 depend from claim 25 and contain all of its limitations. For at least the reasons stated above, Applicant respectfully requests the withdrawal of the rejection and allowance of the claims.

Claims 60-62 depend from claim 39 and contain all of its limitations. For at least the reasons stated above, Applicant respectfully requests the withdrawal of the rejection and allowance of the claims.

Claim 69 depends from claim 20 and contain all of its limitations. The Examiner has stated that claim 20 is allowable. For at least this reason, Applicant respectfully requests the withdrawal of the rejection and allowance of the claim.

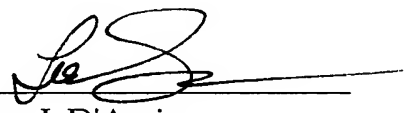
Claims 5, 6, 8-10, 29, 30 and 32-34 stand objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claims and any intervening claims. As discussed above, however, applicant believes that these claims depend from allowable

base claims. Therefore, Applicant respectfully requests the withdrawal of the objection and allowance of the claims.

In view of the above amendment, applicant believes the pending application is in condition for allowance.

Dated: February 16, 2006

Respectfully submitted,

By 

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